IN THE CLAIMS:

Kindly amend claim 1, cancel claims 2-7, and add new claims 8-18 as shown in the following listing of claims, which replaces all previous versions and listings of claims in this application.

1. (currently amended) A method of manufacturing a vertical MOS ~~transistor, comprising~~ transistor comprising:

implanting an impurity of a second conductivity type into a main surface of a semiconductor substrate of a first conductivity type and thermally diffusing the impurity to form a body region of the second conductivity type;

carrying out anisotropic etching ~~for a region in which a trench is intended to be formed on a~~ on a region of the main surface of a semiconductor substrate ~~of a first conductivity type~~ to form ~~the~~ a trench having a plurality of wall surfaces;

forming a gate oxide film over the main surface of the semiconductor substrate ~~of the first conductivity type~~ and along the wall surfaces of the trench;

depositing a polycrystalline silicon layer into the trench and over the main surface of the semiconductor substrate so as to overlie the gate oxide film;

etching the polycrystalline silicon layer so as to remove the polycrystalline silicon layer overlying the main

surface of the semiconductor substrate and so as to remove the polycrystalline silicon layer within the trench to a predetermined depth from the main surface of the semiconductor substrate to form a gate electrode within the trench;

~~implanting an impurity of a second conductivity type into the main surface of the semiconductor substrate of the first conductivity type and thermally diffusing the impurity of the second conductivity type to form a body region of the second conductivity type;~~

implanting an impurity of the first conductivity type into the main surface of the semiconductor substrate to form a source region of the first conductivity type;

implanting an impurity of the second conductivity type into the main surface of the semiconductor substrate to form a body contact region of the second conductivity type;

depositing an intermediate insulating film over the main surface of the semiconductor substrate and the gate electrode;

etching back the intermediate insulating film overlying the main surface of the semiconductor substrate so as to entirely expose the source region and the body contact region ~~constituting~~ forming the main surface of the semiconductor substrate; and

forming a source metal electrode over the main surface of the semiconductor substrate.

2. - 7. (canceled).

8. (withdrawn) A method according to claim 1; wherein the intermediate insulating film comprises a first insulating film; and between the implanting step to form the body contact region and the step of depositing the first insulating film, further comprising the steps of depositing a second insulating film over the main surface of the semiconductor substrate, and removing the first insulating film overlying the main surface of the semiconductor substrate by anisotropic etching to form side spacers made of the second insulating film on the wall surfaces of the trench so as to overly the gate electrode.

9. (withdrawn) A method according to claim 8; wherein the second insulating film comprises a silicon nitride film.

10. (withdrawn) A method according to claim 1; wherein the intermediate insulating film comprises a first insulating film; and between the implanting step to form the body contact region and the step of depositing the first insulating film, further comprising the steps of depositing a second insulating film in a thickness so as to completely fill the trench and so as to overly and flatten the main surface of the semiconductor substrate, and etching back the second

insulating film so as to remove the second insulating film overlying the main surface of the semiconductor substrate and so as to leave the second insulating film within the trench.

11. (withdrawn) A method according to claim 10; wherein the second insulating film comprises a silicon nitride film.

12. (withdrawn) A method according to claim 10; wherein the thickness of the second insulating film falls within a range of 0.3 to 1.0 μm.

13. (withdrawn) A method according to claim 12; wherein the second insulating film comprises a silicon nitride film.

14. (new) A method according to claim 1; wherein the etching back step includes the step of etching back the intermediate insulating film to planarize the main surface of the semiconductor substrate; and wherein the step of forming the source metal electrode comprises the step of forming the source metal electrode as a planar structure.

15. (new) A method according to claim 1; wherein the step of forming the source metal electrode comprises the step of forming the source metal electrode as a planar structure over the main surface of the semiconductor substrate.

16. (new) A method according to claim 1; wherein the step of forming the source metal electrode comprises the step of forming the source metal electrode as a planar structure so as to cover the entire main surface of the semiconductor substrate.

17. (new) A method according to claim 1; wherein the step of forming the source metal electrode comprises the step of forming the source metal electrode as a planar structure so as to increase a contact area between the source metal electrode and the source and body contact regions to thereby substantially reduce a resistance therebetween.

18. (new) A method according to claim 17; wherein the etching back step includes the step of etching back the intermediate insulating film so as to planarize the main surface of the semiconductor substrate to facilitate formation of the source metal electrode as a planar structure over the main surface of the semiconductor substrate.